ABSTRACT OF THE DISCLOSURE

The present invention relates to a method of forming damascene pattern in a semiconductor device, and the method includes forming an insulating layer on a bottom wiring, forming via holes exposing a part of the bottom wiring by removing the insulating layer selectively, filling insides of the via holes to a prescribed thickness, forming an anti-reflection layer on the via holes and the insulating layer, forming a mask pattern for trench etching on the insulating layer on which the anti-reflection layer is formed, and forming a damascene pattern using the mask pattern for trench etching. CD uniformity is improved by minimizing change of the critical dimension of the damascene pattern, thereby increasing reliability of the semiconductor device.